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EXAMINER	
STIGLIC, RYAN M	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,809	TAKATA, YUKARI	
	Examiner	Art Unit	
	Ryan M. Stiglic	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-9 and 11-13* is/are rejected.

7)☒ Claim(s) *4,10,14 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-15 are pending and have been examined.

2. Claims 1-3, 5-9, 11-13 are rejected.

3. Claims 4, 10, and 14-15 are objected to.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butta' et al. (US 6633939 B2) in view of Watts (US 6647449 B1).

For the claims below the Examiner has understood "priority information" to mean information sent from a master device referring to the priority value of a device.

For claim 1:

1. An arbitration circuit for arbitrating bus access requests presented from a plurality of bus masters connected through a shared bus, comprising: a priority check block receiving multiple pieces of priority information outputted respectively from said plurality of bus masters, for comparing said pieces of priority information and specifying masters with a highest priority so as to output a check result; and a round robin block, said round robin block comprising, a round

robin control unit for determining, through a round robin algorithm, a priority order of the bus access requests from said plurality of bus masters, a round robin masking unit for masking data of said check result with mask data to output a masked check result, said mask data being generated on the basis of said priority order, and a final selection unit for selecting a bus master whose bus access request should be accepted on the basis of said masked check result and said check result.

Butta' teaches an arbitration circuit (Fig. 3, A) for arbitrating requests from a plurality of master devices. Priority information (priority 1, priority 2, and priority 3 of Fig. 3) arrive from requesting master devices portraying the relative priority of each device (col. 3, ll. 4-8). The arbitration circuit **A** acts as a priority check block such that it receives multiple pieces of priority information (col. 3, ll. 4-8), compares said pieces of priority information (col. 4, line 6 – col. 5, line 23), and specifies masters with a highest priority so as to output a check result/grants (col. 3, ll. 24-28; col. 4, ll. 52-56). Butta however fails to teach of ordering requests such that upon completion of a first competing request, a second request may be granted.

Watts teaches an improved round robin arbitration block (Fig. 2, 22) for use in computer networks (buses) (col. 1, ll. 5-18). The round robin block contains a round robin control unit (Fig. 4, 44) that determines, through a round robin algorithm, a priority order of access requests (col. 3, ll. 54-65). The round robin control unit 44 receives as input a "recently serviced vector" which is used to create a "mask vector" representing the next highest priority request that may be granted in a round robin fashion. That is to say the round robin control unit 44 preserves the round robin algorithm by proceeding to grant priorities from highest value to lowest value with the use of the "mask vector". Watts also teaches a round robin masking unit (Fig. 3 and 4, 38),

which masks check results by using the priority order ("mask vector") (col. 3, ll. 13-22). Lastly Watts teaches a final selection unit (Fig. 2, 26) for selecting a master whose access request should be accepted based on the masked check result (Fig. 4, 48) and the check result (Fig. 3 and 4, 36).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the round robin circuitry of Watts into the variable priority arbitration system of Butta' such that a variable priority arbitration system is formed with an improved round robin scheduling algorithm that provides a shorter propagation delay and reduces the number of logic gates.

For claim 2:

Butta' teaches, the arbitration circuit according to claim 1, wherein said priority check block comprises: a plurality of first-stage check circuits each receiving two pieces of said priority information as a set, for comparing said two pieces of priority information and outputting a higher priority information as an output priority (Fig. 3, stages A1 and A2; col. 2, ll. 65-66; col. 3, ll. 4-23; col. 3, line 33 – col. 4, line 51); and at least one next-stage check circuit receiving two, as a set, of said plurality of output priorities from said first-stage check circuits, for comparing said two output priorities and specifying masters with a highest priority (Fig. 3, stage A3; col. 2 line 67; col. 3, ll. 24-28; col. 4, ll. 52-56).

For claim 3:

The arbitration circuit according to claim 1, wherein said check result and said mask data are each multi-bit data in which individual bits are assigned respectively to said plurality of bus masters (col. 3, ll. 3-4; where each request represents a master), said mask data masks a bit or bits of higher-order than a bit that is assigned to a master with a highest-priority order (col. 3, ll. 13-22; col. 3, ll. 54-65), and said round robin masking unit performs a logical operation (AND) with the data of said check result and said mask data to obtain said masked check result (col. 3, ll. 13-22; col. 3, ll. 54-65),.

6. Claims 5-8 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butta' et al. (US 6633939 B2) in view of Kurth (US 6880028 B2).

For claim 5:

Butta teaches a data processing system having an arbitration circuit (Fig. 3, A) that receives multiple pieces of priority information (Fig. 3, priority 1, priority 2, or priority 3; col. 3, ll. 4-8) outputted respectively from a plurality of bus masters connected through a shared bus, so as to arbitrate bus access requests (col. 3, line 33 – col. 4, line 56), wherein said plurality of bus masters each comprise a priority generating circuit for generating the priority information (The arbiter **A** of Fig. 3 shows priority information signals transmitted from initiators [col. 3, ll. 4-8], therefore inherently teaching a priority generating circuit for each initiator/master). Butta however fails to teach dynamically changing the priority of a master device.

Kurth teaches a system and method for dynamically determining/varying the priority of requests (abstract). Kurth teaches a priority generating circuit (Fig. 2, 202-206) wherein each of said priority generating circuit ups the level of said priority information when a bus access request from the corresponding bus master is unaccepted (col. 1, ll. 53-55; col. 5, ll. 17-27).

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the dynamic priority ability of Kurth into the arbitration circuit of Butta so that the initiators are given the ability to dynamically change the priority of its own requests thus preventing the master from being starved from access to the resource.

For claim 6

The data processing system according to claim 5, wherein each said priority generating circuit comprises a priority up circuit for, when a bus access request was unaccepted with an outputted piece of priority information (Fig. 3, priority 1, priority 2, or priority 3; col. 3, ll. 4-8), adding or subtracting a given value to or from said outputted piece of priority information, so as to set a new piece of priority information (col. 5, ll. 17-27; The priority up circuit is implied from "the agent *increases* the priority level", thus teaching the adding of a given value to said outputted piece of priority information.).

For claim 7:

The data processing system according to claim 6, wherein each said priority generating circuit further comprises a priority changing quantity setting register for setting said given value. The

invention of Kurth teaches dynamically changing the priority by a constant quantity (col. 1, ll. 29-47; col. 3, ll. 31-55). Although not explicitly stated, the Examiner understands a quantity setting register is present in the invention of Kurth. The priority of the master devices of Kurth changes by 1 each time a threshold is reached or a timer has expired. It is therefore obvious that a quantity setting register with a stored value of 1 is inherently present in the master devices of Kurth.

For claim 8:

The data processing system according to claim 6, wherein each said priority generating circuit further comprises a limiting circuit for limiting the priority upping of said priority information (the priority values are *limited* to the maximum and minimum values shown in Fig. 3).

For claim 13:

Butta teaches a data processing system having an arbitration circuit (Fig. 3, A) that receives multiple pieces of priority information outputted respectively from a plurality of bus masters connected through a shared bus, so as to arbitrate bus access requests (col. 3, line 33 – col. 4, line 56), wherein said plurality of bus masters each comprise a priority generating circuit for generating the priority information (The arbiter **A** of Fig. 3 shows priority information signals transmitted from initiators [col. 3, ll. 4-8], therefore inherently teaching a priority generating circuit for each initiator/master).

Kurth teaches a system and method for dynamically determining/varying the priority of requests (abstract). Kurth teaches a condition of a corresponding bus master is changed (col. 1, ll. 39-55), said priority generating circuit outputs one of pieces of priority information that correspond respectively to a plurality of conditions (col. 3, ll. 24-25).

7. Claims 9 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butta' et al. (US 6633939 B2) in view of Kenny (6393506 B1).

For claim 9:

Butta teaches a data processing system having an arbitration circuit (Fig. 3, A) that receives multiple pieces of priority information outputted respectively from a plurality of bus masters connected through a shared bus, so as to arbitrate bus access requests (col. 3, line 33 – col. 4, line 56), wherein said plurality of bus masters each comprise a priority generating circuit for generating the priority information (The arbiter **A** of Fig. 3 shows priority information signals transmitted from initiators [col. 3, ll. 4-8], therefore inherently teaching a priority generating circuit for each initiator/master) and said priority generating circuit outputs one of pieces of priority information. Butta however fails to teach of dynamically changing priority based on operating frequency.

Kenny teaches assigning priority based on requesting frequency was well known in the art at the time of the applicant's invention (col. 3, ll. 54-65). By dynamically varying the priority of devices over time, arbitration fairness is ensured.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to implement the statistical weighting priority of Kenny into the arbitration system of Butta' such that priority is dynamically allocated to masters as these weightings (operating frequencies) change over time thus providing a fair arbitration scheme.

For claim 11:

The data processing system according to claim 9, wherein said priority generating circuit comprises an adding/subtracting circuit for adding or subtracting a given value to or from reference priority information to set a new piece of priority information. As stated above with respect to claim 9 above, Kenny teaches a statistical weighting priority scheme which assigns a higher priority value to a master device requesting at a higher frequency (col. 3, ll. 54-65). The statistical weighting priority scheme must inherently involve some means of adding/subtracting a given value to a reference priority to achieve the solution of the new weighted priority value.

For claim 12:

The data processing system according to claim 11, wherein said priority generating circuit further comprises a limiting circuit for limiting a maximum value and a minimum value of said new priority information. The Examiner respectfully submits that a limiting circuit must inherently be present in any dynamically alterable priority arbitration system because priorities of devices in a system must be constrained between a given range (i.e. 0-15 or 0-3). Therefore

the dynamically changing statistical weighting priority scheme of Kenny must limit the priority of a device to either the maximum or minimum value.

Allowable Subject Matter

8. Claims 4, 10, and 14-15 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

For claim 4:

While the idea of a separate mask and check results is not novel, it is their orientation to a final selection unit that is novel. The Examiner was unable to find references teaching placing a mask and a check result into a single storage device where the mask check result resided in the high-order portion and the check result resided in the low order portion of the storage device. Watts teaches a multiplexer that receives both the check result and the mask check result (Fig. 4), but does not place the mask check result in the high order bits while the check result resides in the low order bits. Instead Watts teaches a reduction OR (Fig. 4, 50) that results in the selection of the check result bits if the mask check result contains no set bits. The reduction OR reduces the amount of searching for the first active bit by omitting either the check result or the mask check result. Therefore the prior art of record does not teach or suggest combining both the check result and the mask check result into a single string of bits in order to locate the first active request.

For claim 10:

It is common in the art for an arbitration circuit to contain a plurality of priority registers, where each register refers to a master device. However, it is uncommon in the art to have a plurality of priority registers in an initiator device where each register corresponds to an operating frequency of the initiator device. The invention of Kenny teaches varying the priority of the requesting master based on the operating frequency but fails to teach a plurality of priority registers where each register contains a priority value for a given operating frequency. The Examiner was unable to find prior art that taught or suggesting creating a plurality of priority registers where each priority register corresponds to an operating frequency of the initiator device.

For claim 14:

It is common in the art for an arbitration circuit to contain a plurality of priority registers, where each register refers to a master device. However, it is uncommon in the art to have a plurality of priority registers in an initiator device where each register corresponds to a condition of said bus master. As previously stated the invention of Kenny varies the priority of the requesting master on the *condition* that the operating frequency of the device increases or decreases by changing the value of the priority value and not selecting from a plurality of priority registers that are set *in advance*. Furthermore Kurth teaches dynamically varying the priority of a master device on the *condition* of either a timer or the work request queue. Kurth however does not teach selecting a priority register from a plurality of priority registers corresponding to the condition, which occurred. The Examiner was unable to find prior art that taught or suggesting creating a plurality of priority registers where each priority register corresponds to a condition of the initiator device.

For claim 15:

The Examiner was unable to find prior art or suggestions to combine prior art that taught changing the priority of a master device on the conditions of:

- Detecting a branch instruction for fetching an instruction from a branch destination
- An instruction queue for said CPU is vacant
- **AND** a condition in which a store buffer in said CPU is full and data to be stored is waiting.

The Examiner is aware of prior art that dynamically changes priority based on the condition of outstanding requests (i.e. store buffer fullness) but was unable to find prior art that taught or suggested the combination of all three conditions listed above.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Zulian teaches a masking arbiter that keeps track of the last granted requests.
- Cohen teaches branching instructions are a high-priority request.
- Stanton and Revilla teach master devices issuing priority information with their requests.
- Hogg teaches aging requests that are unaccepted.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan M. Stiglic whose telephone number is 571.272.3641. The examiner can normally be reached on Monday-Thursday (6:00-3:30) and Friday (6:00-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 571.272.3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RMS

PAUL R. MYERS
PRIMARY EXAMINER